Atty. Docket No.: 3175-Z

2184
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9-28-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Laung-Terng Wang et al
Serial No. 10/086,214
Filed: March 27, 2002 Group Art Unit 2184
For: Method and Apparatus for Diagnosing Failures in an Integrated Circuit Using Design-for-Debug (DFD) Techniques

INFORMATION DISCLOSURE STATEMENT

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Information Disclosure Statement is submitted:

[X] under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first Office action on the merits; whichever occurs last.)

[] under 37 CFR 1.97(c) together with either a:
[] Certification under 37 CFR 1.97(e), or
[] a $240.00 fee under 37 CFR 117(p), or
(After the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first.)

[] under 37 CFR 1.97(d) together with either a:
[] Certification under 37 CFR 1.97(e), and
[] a petition under 37 CFR 1.97(d)(2)(ii), and
[] a $130.00 petition fee set forth in 37 CFR §117(i)(1).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee.)

Applicant(s) submits herewith Form PTO 1449-Information Disclosure Citation together with copies of patents, publications or other information of which applicant(s) is aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

The relevance of the attached references is that this is the closest art of which applicant(s) is aware.

Applicant(s) submits that the above references taken alone or in combination neither anticipate nor render obvious the present invention. Consideration of the foregoing in relation to this application is respectfully requested.

Respectfully submitted,

Jim Zegeer

Jim Zegeer, Reg. No. 18,957
Attorney for Applicant(s)

Attachments:
Form PTO-1449 and cited references

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Date: June 14, 2002

In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.

FORM PTO-1449 (MODIFIED) U.S. Department of Commerce Patent and Trademark Office	ATTY. DOCKET NO. 3175-Z	SERIAL NO. 10/086,214
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANT Laung-Terng Wang et al	
	FILING DATE February 27, 2002	GROUP 2184

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,488,688	01/1996	Gonzales et al	714	34	
		5,491,793	02/1996	Somasundaram et al	714	45	
		5,544,311	08/1996	Harenberg et al	714	40	
		5,724,505	03/1998	Argade et al	714	45	
		5,828,824	10/1998	Swoboda	714	25	
		5,828,825	10/1998	Eskandari et al	714	27	
		5,881,067	03/1999	Narayanan et al	714	726	
		6,249,893	06/2001	Rajsuman et al	714	741	
		6,308,290	10/2001	Forlenza et al	714	724	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		J. Ghosh-Dastidar et al, "A Rapid and Scalable Diagnosis Scheme for BIST Environments with a Large Number of Scan Chains," Proc., *IEEE VLSI Test Symposium*, pp. 79-85, 2000. /COPY ENCLOSED/
		M. Abromovici et al, *Digital Systems Testing and Testable Design*, Computer Science Press, New York, 1990 /COPY UNAVAILABLE/
		M. Crouch, *Design-for-Test for Digital IC's and Embedded Core Systems*, Prentice Hall PTR, New Jersey, 2000 /COPY UNAVAILABLE/
		Nadeau-Dostie, *Design for At-Speed Test, Diagnosis and Measurement*, Kluwer Academic Press, Norwell, MA, 2000 /COPY UNAVAILABLE/
		IEEE, *IEEE Standard Test Access port and Boundary-Scan Architecture: IEEE Std 1149.1-1990 (Includes IEEE Std 1149.1a-1993)*, IEEE Computer Society, New York, Oct. 21, 1993 /COPY UNAVAILABLE/

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.